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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/574,798	12/11/2006	Bernard Aspar	288918US6PCT	2578

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EXAMINER	
SLUTSKER, JULIA	

ART UNIT	PAPER NUMBER
2891	

NOTIFICATION DATE	DELIVERY MODE
05/11/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/574,798	ASPAR ET AL.	
	Examiner	Art Unit	
	JULIA SLUTSKER	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *68-72,74-79,85,87-93 and 98* is/are pending in the application.

4a) Of the above claim(s) *69-72* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *68,74-79,85,87-93 and 98* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 July 2010* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/21/2011*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/21/2011 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 88 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 88 recites the limitation "the eliminating takes place before a previous surface penetration of the first wafer." This limitation renders the claim indefinite since it is unclear how eliminating can take place before "a previous" surface penetration.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 68, 78, 85, 87, 90-93, and 98 are rejected under 35 U.S.C. 102(b) as being anticipated by Aspar (US 2003/0077885).

Regarding claim 68, Aspar discloses a method of assembling a first wafer onto a second wafer, the first wafer (Fig.2F, numerals 17, 15) including a lower layer having no circuits and components (Fig. 2F, numeral 17) and an upper transplant layer (Fig.2F, numeral 15) arranged at least under the frontal side of the first wafer (Fig.2F, numeral 15), the transplant layer having at least one of circuits and components (Fig.2C, numeral 20), comprising: eliminating material from the upper transplant layer and the lower layer from a frontal side of the first wafer in a peripheral area of the first wafer (Fig.2G,[0075]) over a thickness less than an entire thickness of the first wafer (numerals 15, 17), but greater than an entire thickness of the upper transplant layer (numeral 15), after the at least one of circuits and components (20) have been formed in the upper transplant layer (15); and assembling the upper transplant layer of the first wafer(Fig.2I) onto a second wafer (Fig.2I, numeral 22) after said eliminating material (Fig.2G).

Regarding claim 76, Aspar discloses additional eliminating of material after said assembling of the first and second wafers (Fig.2T, [0077]).

Regarding claim 78, Aspar discloses the eliminating is performed over a width, measured on a plane parallel to the frontal side of the first wafer, at least equal to a width of a zone of the first wafer which can not, without said step of eliminating, be assembled with the second wafer (Fig.2G).

Regarding claim 85, Aspar discloses that the assembling the first and second wafers is performed via molecular adhesion ([0074]).

Regarding claim 87, Aspar discloses that the eliminating takes place after a previous surface preparation of the first wafer for a purpose of assembling ([0072]).

Regarding claim 90, Aspar discloses the first and the second wafers is made in a semiconductor material ([0078]).

Regarding claim 91, Aspar discloses at least one of the first and the second wafers is made in silicon or in a III-V type semiconductor material (claim 22).

Regarding claim 92, Aspar discloses that at least one of the first and second wafers is made in Germanium or piezoelectric material (claim 18).

Regarding claim 93, Aspar discloses that the eliminating is performed in a regular manner around the first wafer (Fig.2G).

Regarding claim 98, Aspar discloses additional eliminating of material from the first wafer from a lateral side of the first wafer over a length L2 that removes some material of the upper transplant layer (Fig.2I).

6. Claims 68 and 89 are rejected under 35 U.S.C. 102(b) as being anticipated by Joly (US 6, 159, 323).

Regarding claim 68, Joly discloses a method of assembling a first wafer onto a second wafer, the first wafer (Fig.2 numeral 10) including a lower layer having no circuits and components (Fig. 2, lower part of (10)) and an upper transplant layer (Fig.2, upper part of (10)) arranged at least under the frontal side of the first wafer (10), the transplant layer having at least one of circuits and components (12), comprising: eliminating material from the upper transplant layer and the lower layer from a frontal side of the first wafer in a peripheral area of the first wafer (Fig. 2, numeral 26) over a thickness less than an entire thickness of the first wafer (10)), but greater than an entire thickness of the upper transplant layer (upper part of (10)), after the at least one of circuits and components (12) have been formed in the upper transplant layer (upper part of (10)); and assembling the upper transplant layer of the first wafer(Fig.4, upper part of (10)) onto a second wafer (Fig.4, numeral 33) after said eliminating material (Fig.4, numeral 26).

Regarding claim 89, Joly discloses that the eliminating is performed via chemical etching (column 5, lines 47-50).

7. Claims 68, 74, 75, and 89 are rejected under 35 U.S.C. 102(e) as being anticipated by Nemoto (US 7, 195, 988).

Regarding claim 68, Nemoto discloses a method of assembling a first wafer onto a second wafer, the first wafer (Fig.8I, numeral 50) including a lower layer having no circuits and components (Fig. 8II, lower part of (50)) and an upper transplant layer (Fig.8II, upper part of (50)) arranged at least under the frontal side of the first wafer (Fig.28II, numeral 50), the transplant layer having at least one of circuits and

components (Fig.8II, numeral 2), comprising: eliminating material from the upper transplant layer and the lower layer from a frontal side of the first wafer in a peripheral area of the first wafer (Fig. 8III) over a thickness less than an entire thickness of the first wafer (50)), but greater than an entire thickness of the upper transplant layer (upper part of (50)), after the at least one of circuits and components (2) have been formed in the upper transplant layer (upper part of (50)); and assembling the upper transplant layer of the first wafer(upper part of (50)) onto a second wafer (Fig.8IV, numeral 3) after said eliminating material (Fig.8III).

Regarding claim 74, Nemoto discloses the first wafer is chamfered and includes at least a chamfered edge (Fig.8, numeral 50).

Regarding claim 75, Nemoto discloses the eliminating is performed over a width, measured on a plane parallel to the frontal side of the first wafer, at least equal to a width of the chamfered edge, measured on the same plane (Fig.8III).

Regarding claim 89, Nemoto discloses that the eliminating is performed via mechanical etching (column 3, lines 60-67).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 77 and 79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aspar.

Regarding claim 77, Aspar does not disclose the eliminating is performed over a thickness of the first wafer between 1 μm and 100 μm.

Aspar however discloses that eliminating is performed to form trenches to assist in transferring process (column 5, lines 50-55; column 6, lines 51-56).

It would have been however obvious to one of ordinary skill in the art at the time the invention was made to adjust the thickness of the first wafer to be in the claimed range for the purpose of optimizing the transferring process.

Regarding claim 79, Aspar does not disclose that the eliminating is performed over a width, measured on a plane parallel to that of the first wafer of between 100 μm and 5 μm.

Aspar however discloses that eliminating is performed to form trenches to assist in transferring process (column 5, lines 50-55; column 6, lines 51-56).

It would have been however obvious to one of ordinary skill in the art at the time the invention was made to adjust the thickness of the first wafer to be in the claimed range for the purpose of optimizing the transferring process.

10. Claims 68, 74, 75, 77-79, 85, and 87-93 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacNamara (US 6, 841, 848) in view of Kim (US 6, 790, 748).

Regarding claim 68, MacNamara discloses a method of assembling a first wafer onto a second wafer, the first wafer (Fig.4, numeral 9) including a lower layer having no circuits and components (lower part of (9))) and an upper transplant layer (upper part of (9)) arranged at least under the frontal side of the first wafer (9), the transplant layer having at least one of circuits and components (note: (9) is a device layer), comprising:

eliminating material from the upper transplant layer and the lower layer from a frontal side of the first wafer in a peripheral area of the first wafer (Fig. 8, numeral 9; column 9, lines 30-45) over a thickness less than an entire thickness of the first wafer (9)), but greater than an entire thickness of the upper transplant layer (upper part of (9)), and assembling the upper transplant layer of the first wafer(upper part of (9)) onto a second wafer (Fig.10, numeral 30) after said eliminating material (Fig.8).

MacNamara does not discloses that eliminating is performed after the at least one of circuits and components have been formed in the upper transplant layer.

Kim however discloses that eliminating of material (Fig.4, numeral 132) is performed after the at least one of circuits and components (Fig.1, numeral 110) have been formed in the upper transplant layer (Fig.1, upper part of (106)).

It would have been therefore obvious to one of ordinary skill in the art at the time the invention was made to modify MacNamara with Kim to perform eliminating after the at least one of circuits and components have been formed in the upper transplant layer for the purpose of fabrication stacked microelectronic device (Kim, column 3, lines 59-67).

Regarding claim 74, MacNamara discloses that the first wafer is chamfered and includes at least a chamfered edge (Fig.7, numeral 26).

Regarding claim 75, MacNamara discloses that the eliminating is performed over a width, measured on a plane parallel to the frontal side of the first wafer, at least equal to a width of the chamfered edge, measured on the same plane (Fig.8, numeral W).

Regarding claim 77, MacNamara does not disclose the eliminating is performed over a thickness of the first wafer between 1 μm and 100 μm. MacNamara however discloses that eliminating is performed to avoid danger of an unbounded peripheral area being formed around of a composite wafer (column 8, lines 53-60).

It would have been however obvious to one of ordinary skill in the art at the time the invention was made to adjust the thickness of the first wafer to be in the claimed range for the purpose of optimizing the lamination process (MacNamara, column 8, lines 53-60).

Regarding claim 79, MacNamara does not disclose that the eliminating is performed over a width, measured on a plane parallel to that of the first wafer of between 100 μm and 5 μm. MacNamara however discloses that eliminating is performed to avoid danger of an unbounded peripheral area being formed around of a composite wafer (column 8, lines 53-60).

It would have been however obvious to one of ordinary skill in the art at the time the invention was made to adjust the thickness of the first wafer to be in the claimed range for the purpose of optimizing the lamination process (MacNamara, column 8, lines 53-60).

Regarding claim 78, MacNamara discloses that the eliminating is performed over a width, measured on a plane parallel to the frontal side of the first wafer, at least equal to a width of a zone of the first wafer which can not, without eliminating, be assembled with the second wafer (Fig.8, numeral W).

Regarding claim 85, MacNamara discloses that the assembling the first and second wafers is performed via molecular bonding (column 9, lines 50-67).

Regarding claim 87, MacNamara discloses that the eliminating takes place after a previous surface preparation of the first wafer for a purpose of assembling (column 9, lines 15-20).

Regarding claim 88, MacNamara discloses the eliminating takes place before a previous surface penetration of the first wafer for a purpose of assembling or transplanting (column 9, lines 50-55).

Regarding claim 89, MacNamara discloses that the routing is performed via plasma etching (column 9, lines 25-50).

Regarding claim 90, MacNamara discloses that at least one of the first and second wafers is made in a semiconductor material (column 8, lines 1-15).

Regarding claim 91, MacNamara discloses at least one of the first and second wafers is made of silicon (column 8, lines 1-15).

Regarding claim 92, MacNamara discloses at least one of the first and second wafers is made of an insulating material (column 8, lines 1-15).

Regarding claim 93, MacNamara discloses that the eliminating is performed in a regular manner around the first wafer (Fig..8).

Response to Arguments

11. Applicant's arguments with respect to claims 68, 74-79, 85, 87-93, and 98 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JULIA SLUTSKER whose telephone number is (571)270-3849. The examiner can normally be reached on Monday-Friday, 8 a.m.-5 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kiesha Bryant can be reached on (571)-272-1844. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Julia Slutsker/
Examiner, AU 2891

May 2, 2011